Lesson 6

Thermomechanical Measurements for Energy Systems (MENR)

Measurements for Mechanical Systems and Production (MMER)

A.Y. 2015-16

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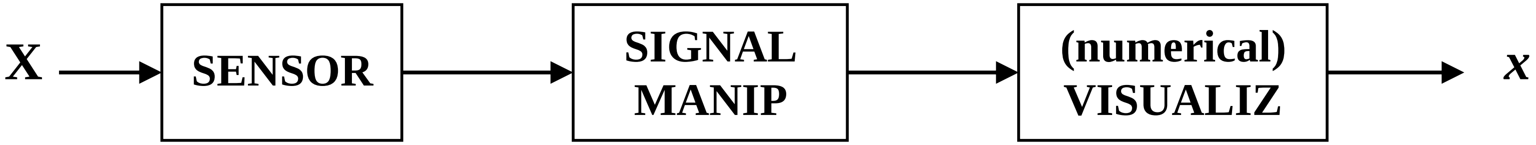
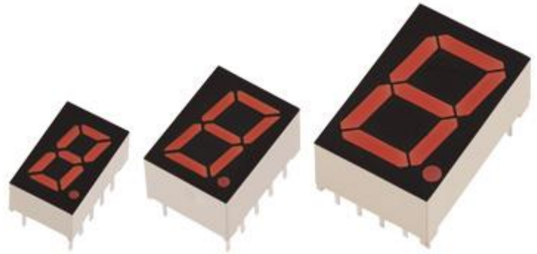
Numerical & Digital instruments :

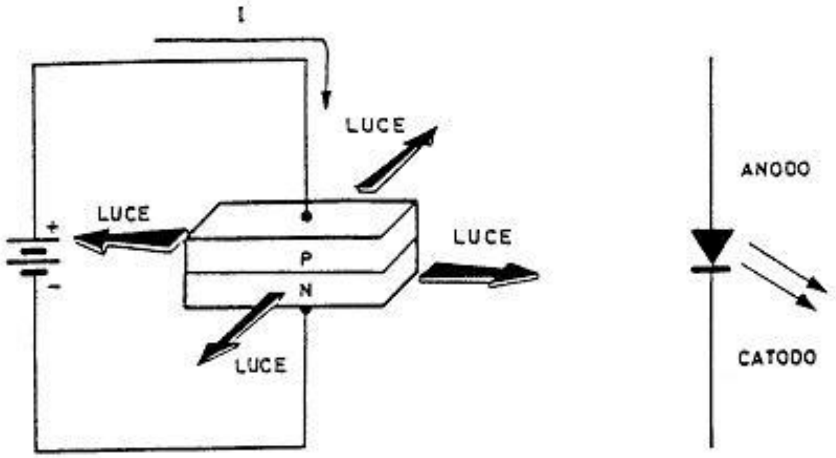
Numerical (and ***digital***) *instruments* display the “measurement” information directly with *numbers* in ***digit format !***



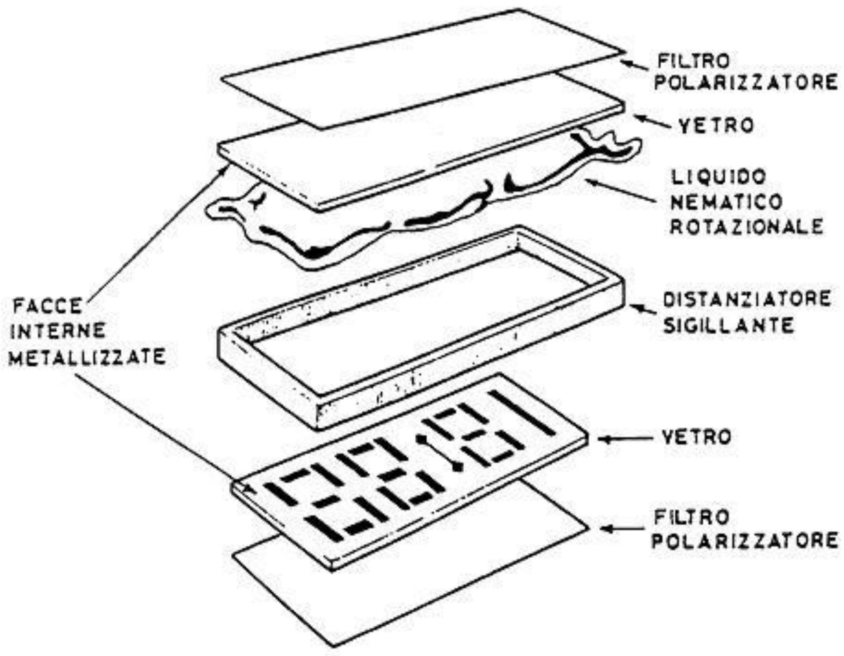


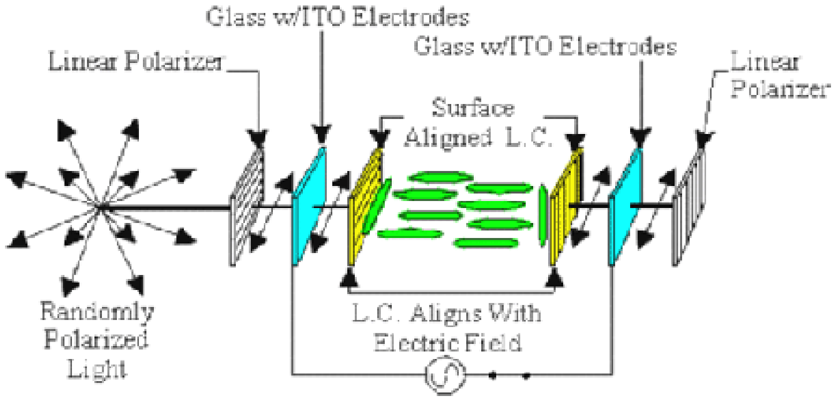
No mechanical indicator;
No indication delay;
No reading errors; …

The first numerical indicators were ***Light Emitting Diodes*** (***LED***) made of *gallium arsenide* (GaS) and *gallium phosphide* (GaP) PN junctions directly polarized !
They use current and, therefore, they heat up … they were highly miniaturized … <u>each diode is one of the seven light emitting bar</u> !

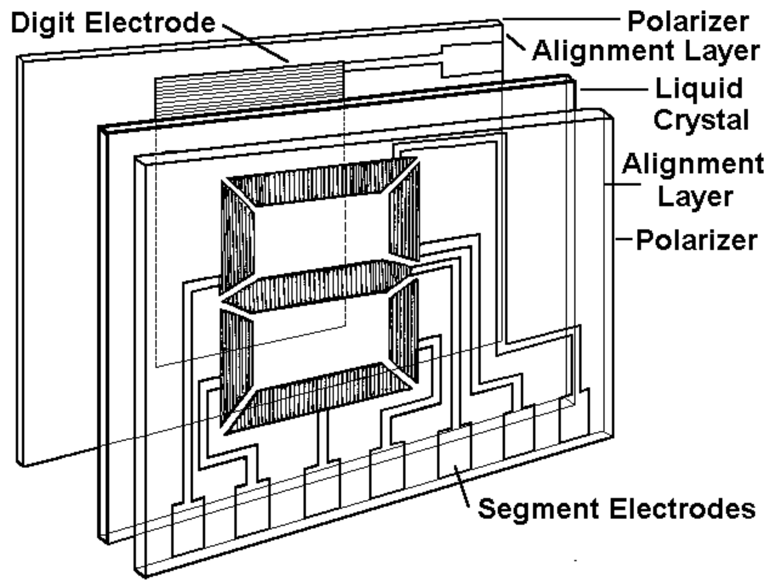


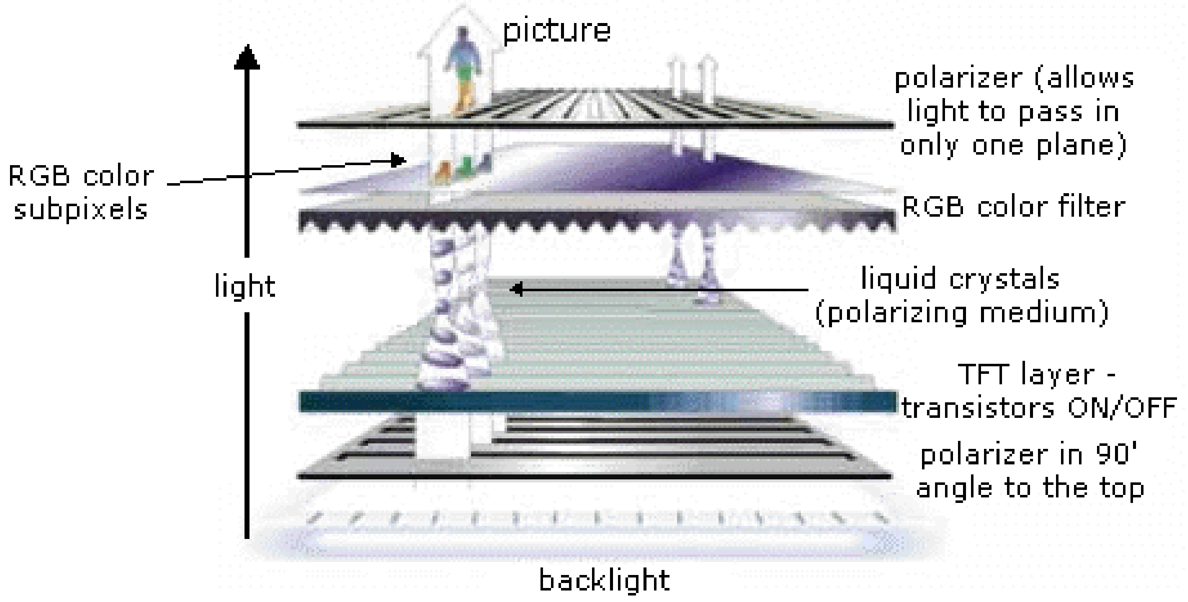
Liquid Cristal Display (**LCD**) are much more efficient, because they DO NOT consume current …



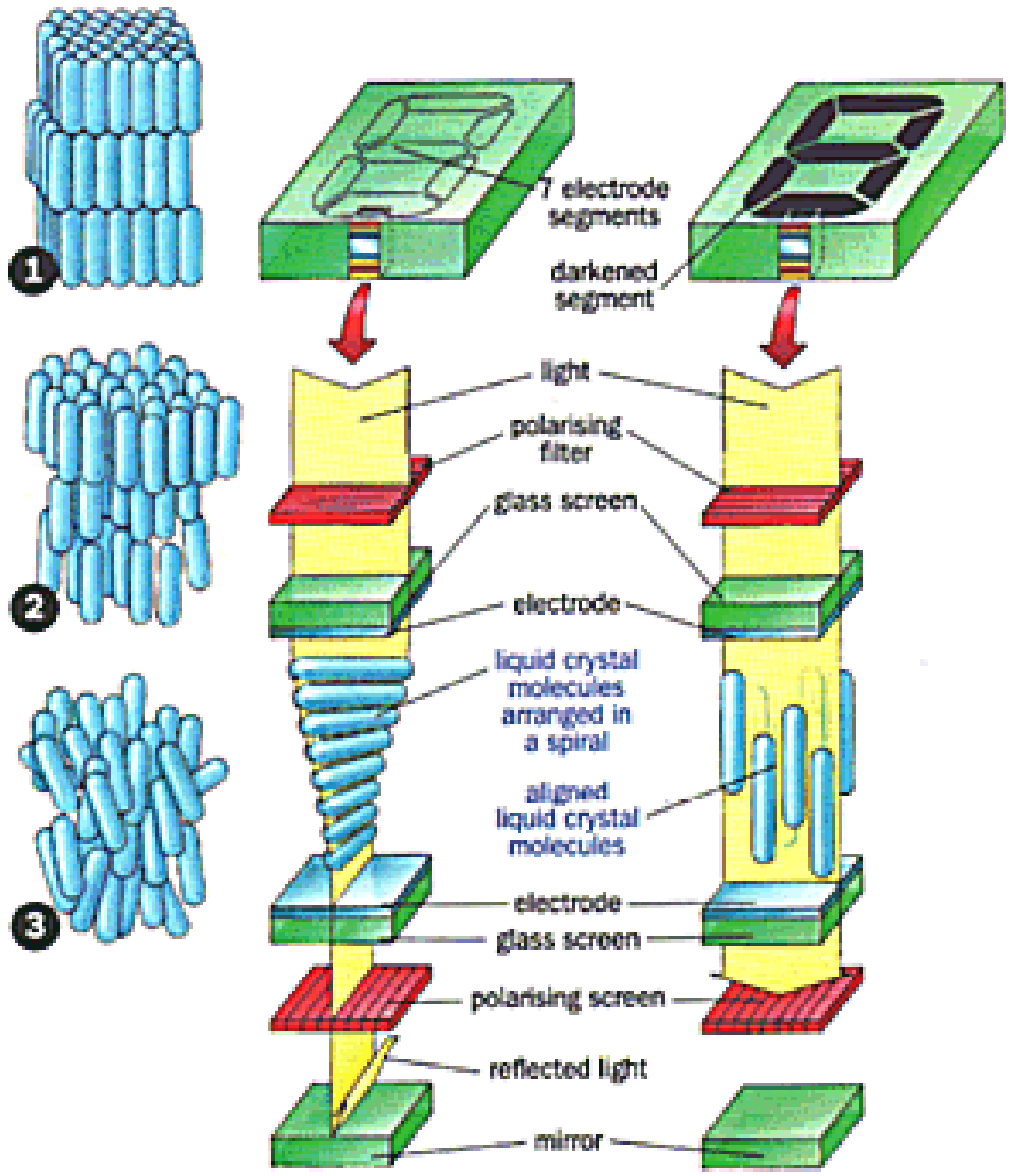


A simple black or white LCD display works by either allowing daylight to be reflected back out at the viewer or preventing it from doing so, in which case the viewer sees a black area.
The liquid crystal is the part of the system that either prevents light from passing through it or not.
The crystal is placed between two polarising filters that are at right angles to each other and together block light. When there is no electric voltage applied to the crystal, it twists light by 90°, which allows the light to pass through the second polariser and be reflected back. But when the voltage is applied, the crystal molecules align themselves, and light cannot pass through the polariser: the segment turns black. Selective application of voltage to electrode segments creates the digits we see.





TFT LCD display



Electronic and Digital Counters:

$$\boxed{N = k_n x^n + k_{n-1} x^{n-1} + \ldots + k_1 x^1 + k_0 x^0 + k_{-1} x^{-1} + \ldots}$$

Generic way of <u>exploding</u> the <u>representation of a number</u> !

$$8725{,}4 = 8 \cdot 10^3 + 7 \cdot 10^2 + 2 \cdot 10^1 + 5 \cdot 10^0 + 4 \cdot 10^{-1}$$

example of a number *N* = 8725,4 expressed in ***decadic base***

$$19 = 1 \cdot 2^4 + 0 \cdot 2^3 + 0 \cdot 2^2 + 1 \cdot 2^1 + 1 \cdot 2^0$$

example of a number *N* = 19 expressed in ***binary base***
in summary form: 1 0 0 1 1

$$147 = 1 \cdot 2^7 + 0 \cdot 2^6 + 0 \cdot 2^5 + 1 \cdot 2^4 + 0 \cdot 2^3 + 0 \cdot 2^2 + 1 \cdot 2^1 + 1 \cdot 2^0$$

example of a number *N* = 147 expressed in ***binary base***
in summary form: 1 0 0 1 0 0 1 1

It is easily seen, that in *binary format* the "coefficients" that are needed (the <u>b</u>inary dig<u>it</u>s : ***bit***) increase rapidly !
A ***bit*** is an <u>elementary information carrier</u> !

However, in the *electronic measurement instrumentation* a special code system is employed: the <u>***BCD code***</u> (***Binary Coded Decimal***) which encodes in binary the *individual decimal* ***digits*** !

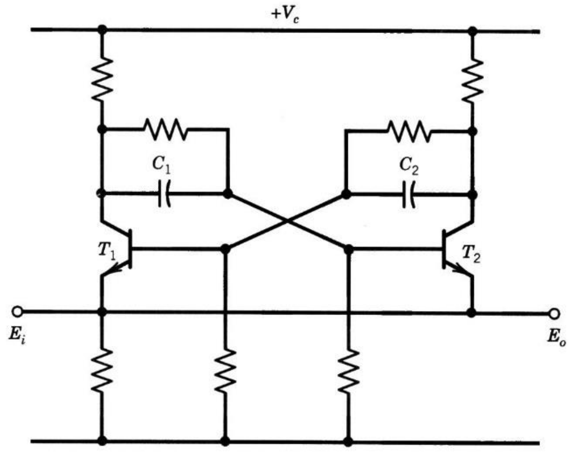
This is a pure binary code that encodes the *ten digits from 0 to 9* with a <u>four bit</u> configuration …
Remember : with "*n* bits" we can count in binary up to $2^n - 1$

Decimal Digit	Four-Bit Binary Equivalent	Binary-Coded Decimal Equivalent
0	0000	0000
1	0001	0001
2	0010	0010
3	0011	0011
4	0100	0100
5	0101	0101
6	0110	0110
7	0111	0111
8	1000	1000
9	1001	1001
10	1010	Illegal
11	1011	Illegal
12	1100	Illegal
13	1101	Illegal
14	1110	Illegal
15	1111	Illegal

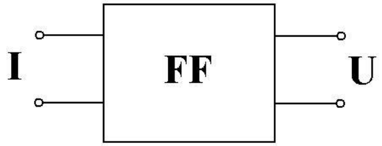
The fundamental basic element for the ***electronic counting*** is the _*astable electronic multivibrator*_ (***FLIP – FLOP***)

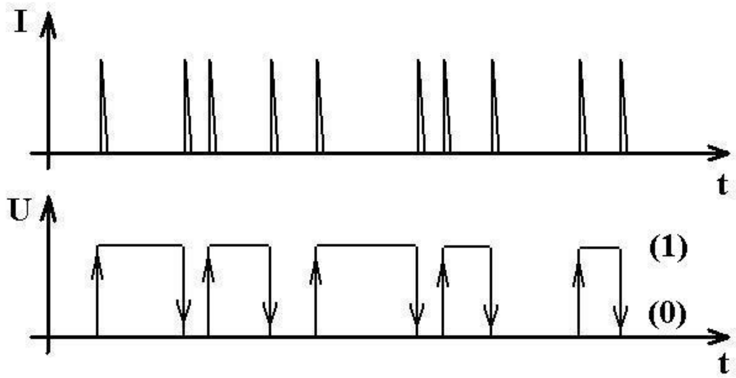
The ***FF*** changes status when it receives a trigger at its input, and "keeps the new status" until a new trigger is received at the input of the device:

Note on the left table:
4 bits = we count up to $2^4 - 1$

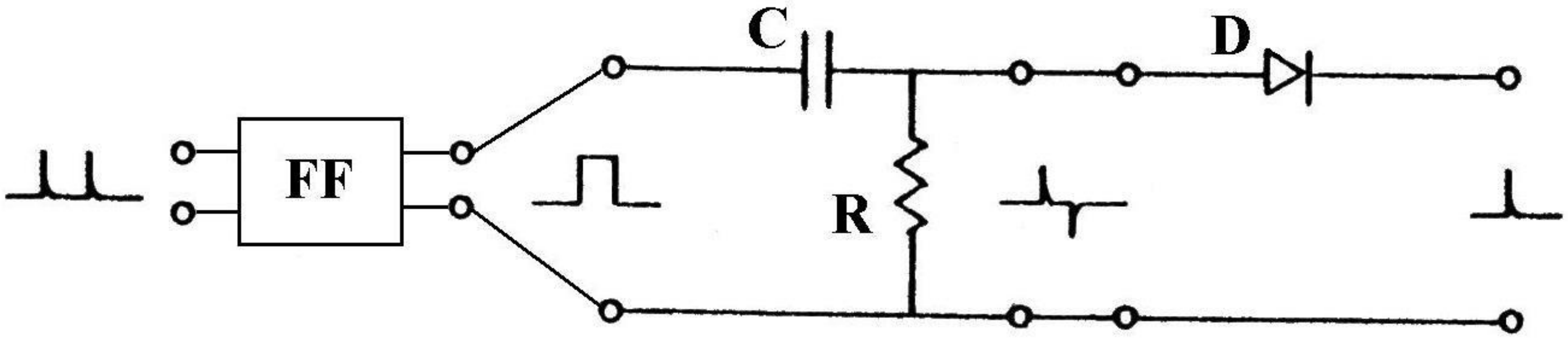


Basic flip-flop circuit.



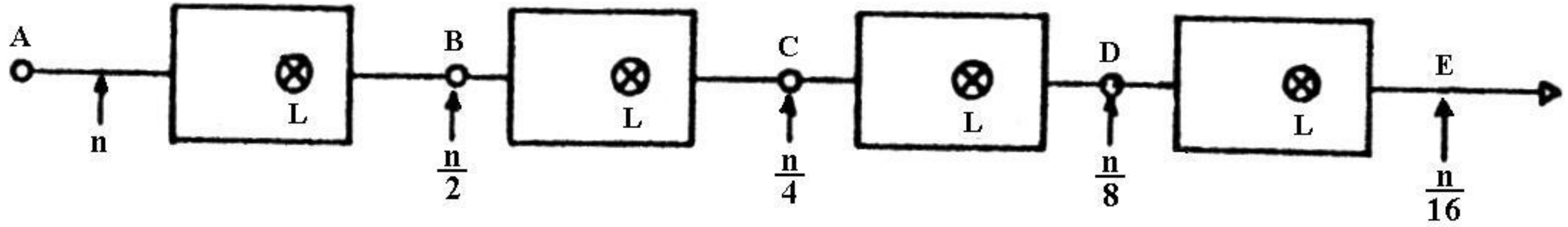


A ***Flip – Flop*** (***FF***) together with a ***CR circuit*** and a ***rectifier diode*** is the "elementary circuit" of the **_BCD counter_ :**



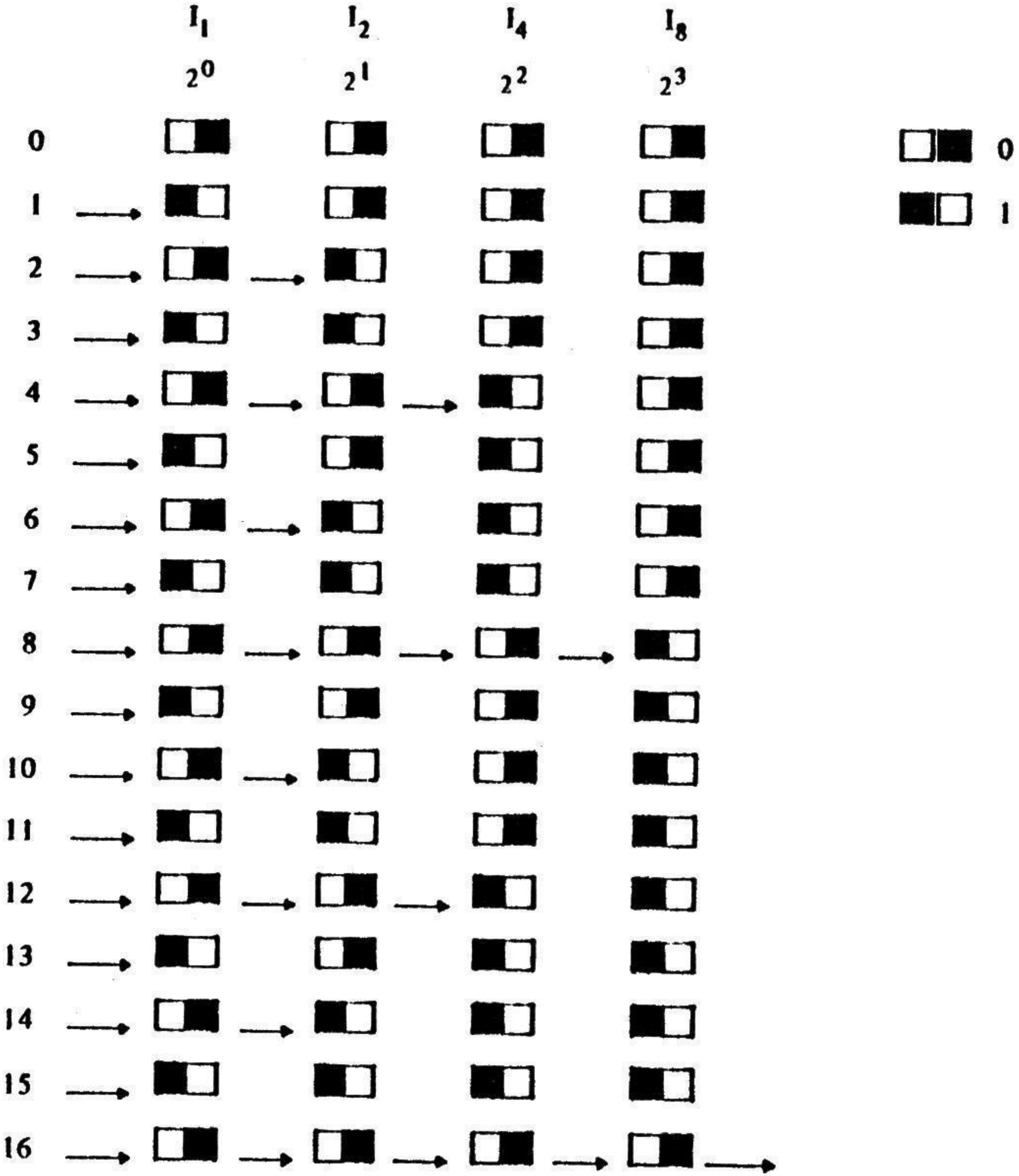
Note that for every two triggers at the circuit input, we have only one trigger at the output !
The circuit *divides by two* the electric triggers received at its input !

If we connect *four of these elementary cells* in series, we have designed the electronic circuit that *counts in the BCD code a single digit* (from 0 to 9) :



Indicators L tell if the FF is in the *High* (X) or *Low (O)* status

n is the number of triggers received at the input !



Note that, to get one trigger at the output we need 16 input triggers … after that, the counter resets to zero again.
We recognize that the 4 Flip Flop (I_1 I_2 I_4 I_8) are the *elementary (**digital**) memory cells* which change the "combination of their status" depending on how many triggers are inputted to the device.
The four cells count in binary code:

$$\boxed{(0;1)\cdot 2^0 + (0;1)\cdot 2^1 + (0;1)\cdot 2^2 + (0;1)\cdot 2^3}$$

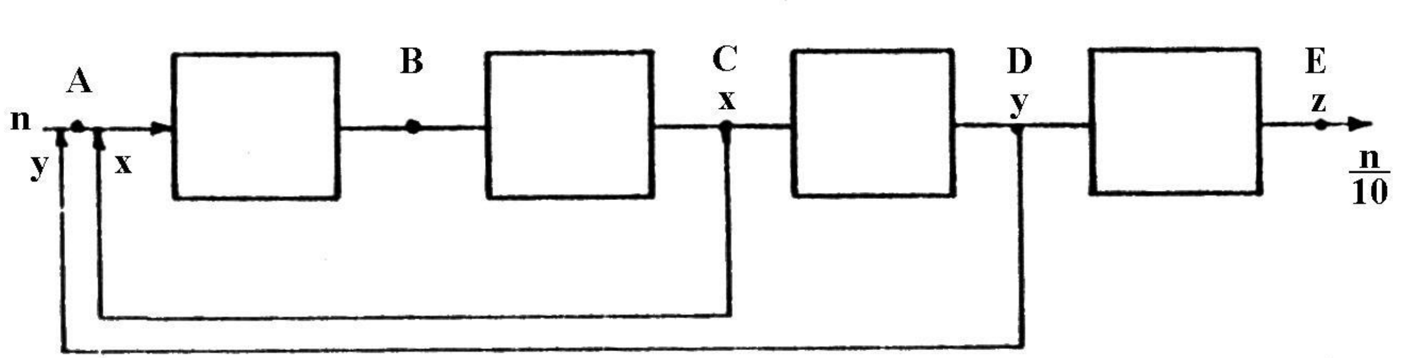
LSB **MSB**

LSB = Least Significant Bit
MSB = Most Significant Bit

examples: 6 = 0 1 1 0
11 = 1 1 0 1
14 = 0 1 1 1

However, to realize the ***BCD counter***, we need the counter to count only up to 9 therefore, the remaining numbers (10 to 15) must be assigned ***illegal value*** … and to realize a decimal counter, we need also one trigger to be outputted every ten input triggers !

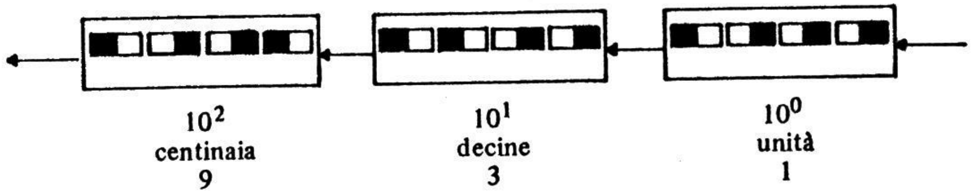
To obtain this result, we have to modify the electronic circuit, speeding up the trigger output by "sending some extra triggers" at the input with a double feedback:



After the "double feedback" we have at the input A: $n+x+y$ triggers and at the feedback point C we have no more $n/4$ triggers, but $\dfrac{n+x+y}{4} = x$

Because it is also $y = x/2$ and $z = y/2$

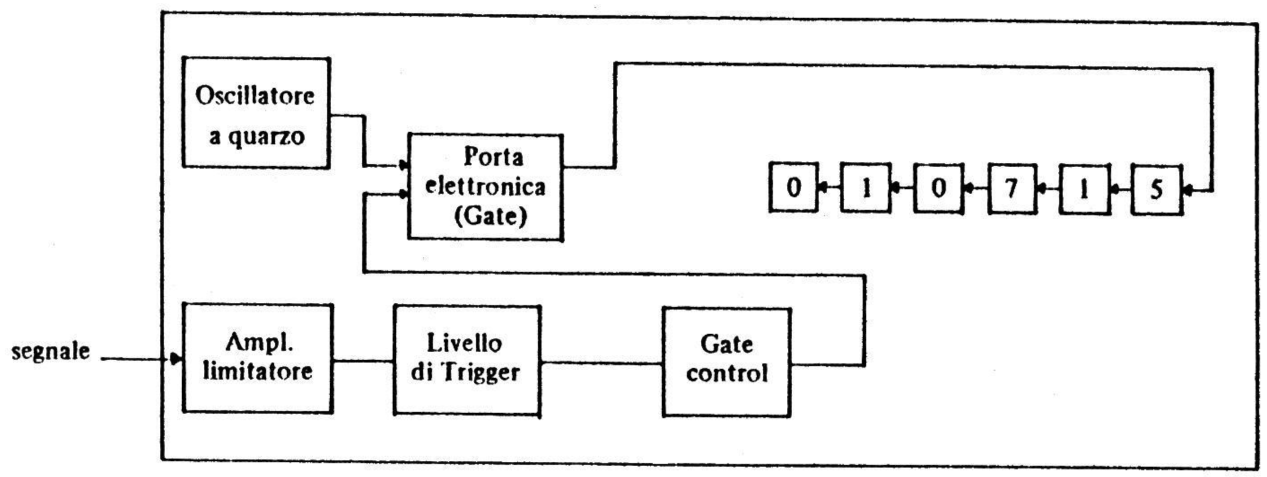
we can write: $\dfrac{n+2y+y}{4} = 2y$ and $n + 3y = 8y$ $n = 5y$ or: $\boxed{z = \dfrac{n}{10}}$ and we reached our result !



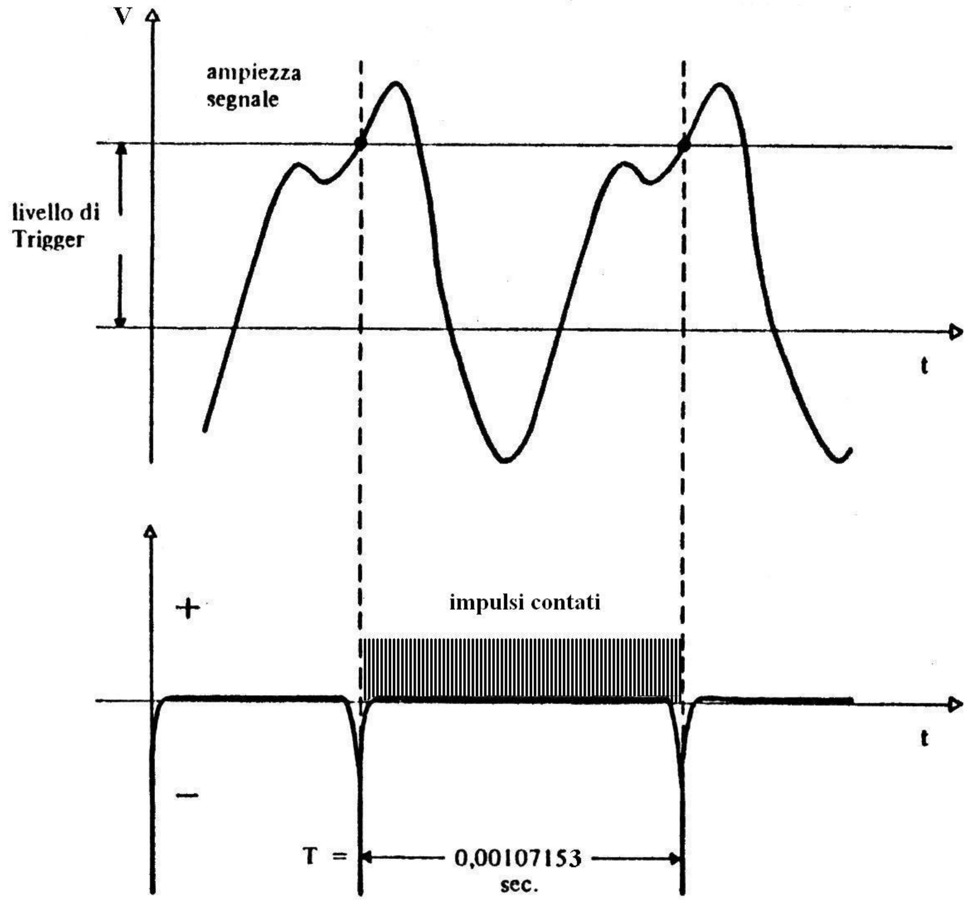
Unità di conteggio decimale

BCD counters with feedback can be "connected in series" so to count decimal numbers but, to be consistent with the *way we read numbers* the circuits must be rotated 180° and the triggers must be inputted from the right side !

Time and Frequency Measurement:



If we connect to the *BCD counter* an electronic gate, a quartz clock, an event input amplifier with a gate control, we can measure with *high resolution* the time between two events:

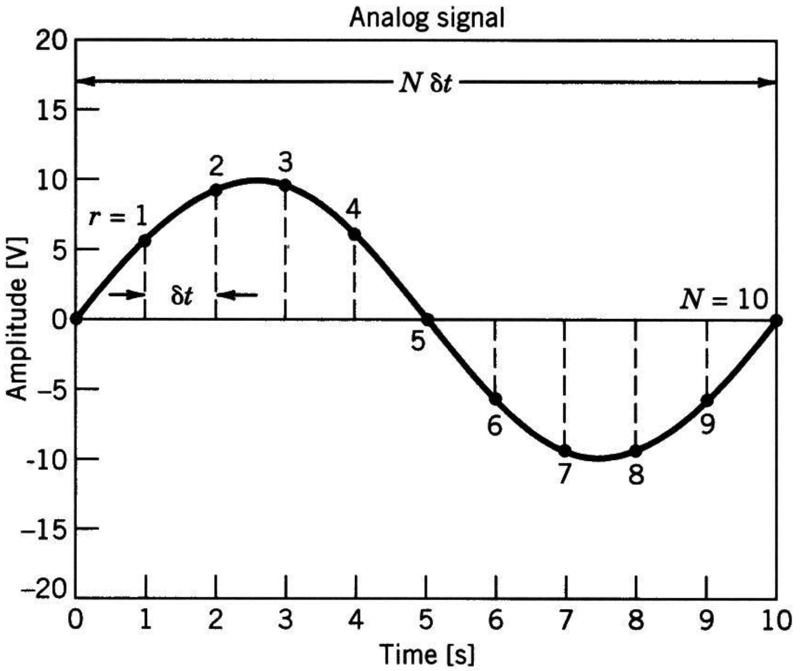


The clock is an ***electronic oscillator*** with a "fairly high" frequency (100 MHz) and is always on.
The gate control opens and closes the gate depending on the input signal level. The triggers produced by the clock pass through the gate and are counted (*n*) by the BCD counter only during the period of time (*t*) for which the gate is open:

$$t = \frac{n}{f_{CLK}} = \frac{107153}{10^8\,Hz} = 0.00107153\ s$$

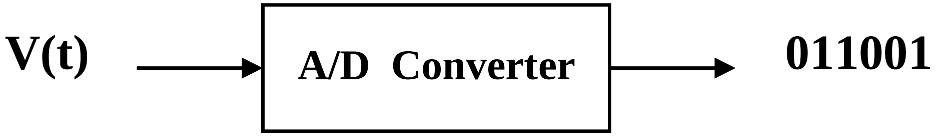
Analog to Digital (**A/D**) Conversion:

Electronic and Digital Counters are fundamental devices for *Analog to Digital* and *Digital to Analog Conversion*



Discrete time signal	
{y(rδt)}	
r	Discrete data
0	0
1	5.9
2	9.5
3	9.5
4	5.9
5	0
6	–5.9
7	–9.5
8	–9.5
9	–5.9
10	0

Analog and discrete representations of a time-varying signal.



Sampling a signal means to "extract" from the analog continuous voltage signal a certain number of voltage values (the ***samples***), measured each other at a regular time distance (the ***sampling period***) !

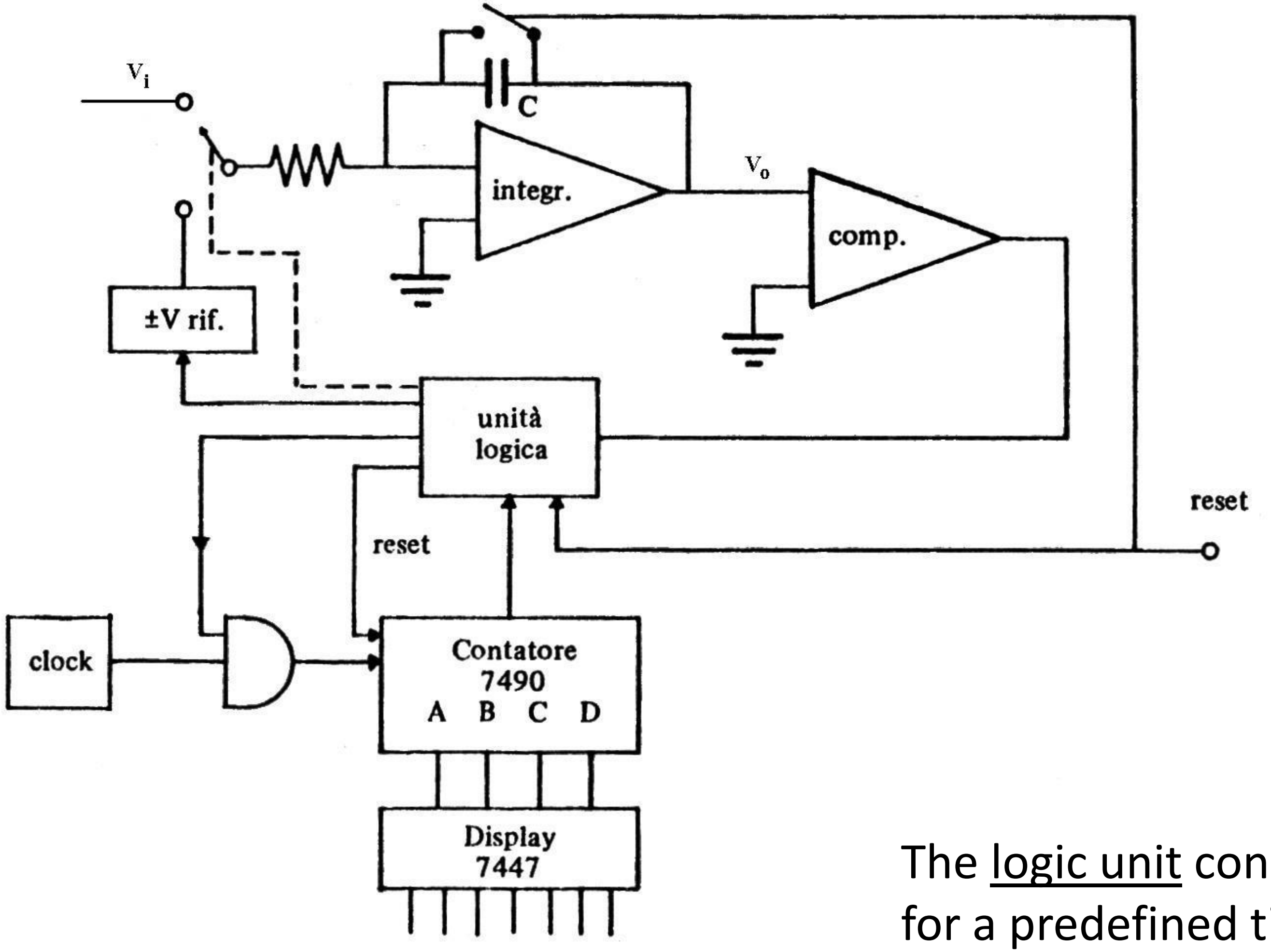
Sampling a signal is always a *loss of information* !

The inverse of the sampling period is the ***sampling frequency*** **:** $f_c = 1/T_c$

If the sampling frequency is not "chosen carefully" the information of the analog measured signal can be completely spoiled !

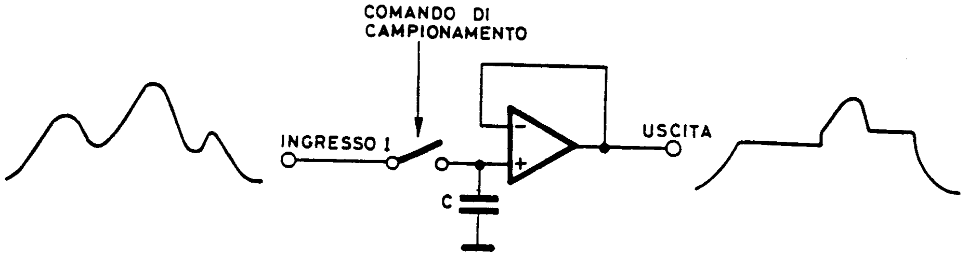
The "sampling" procedure is done by special electronic devices called ***A/D Converters***

Today there are many different types of *A/D converters* employed in so many *appliances of consumer electronics*.
We will study the three most important ***A/D converters for measurement instruments*** :



The ***integrating converter*** or ***voltage to time converter*** is the device which equips all the bench digital voltmeters in the laboratory !

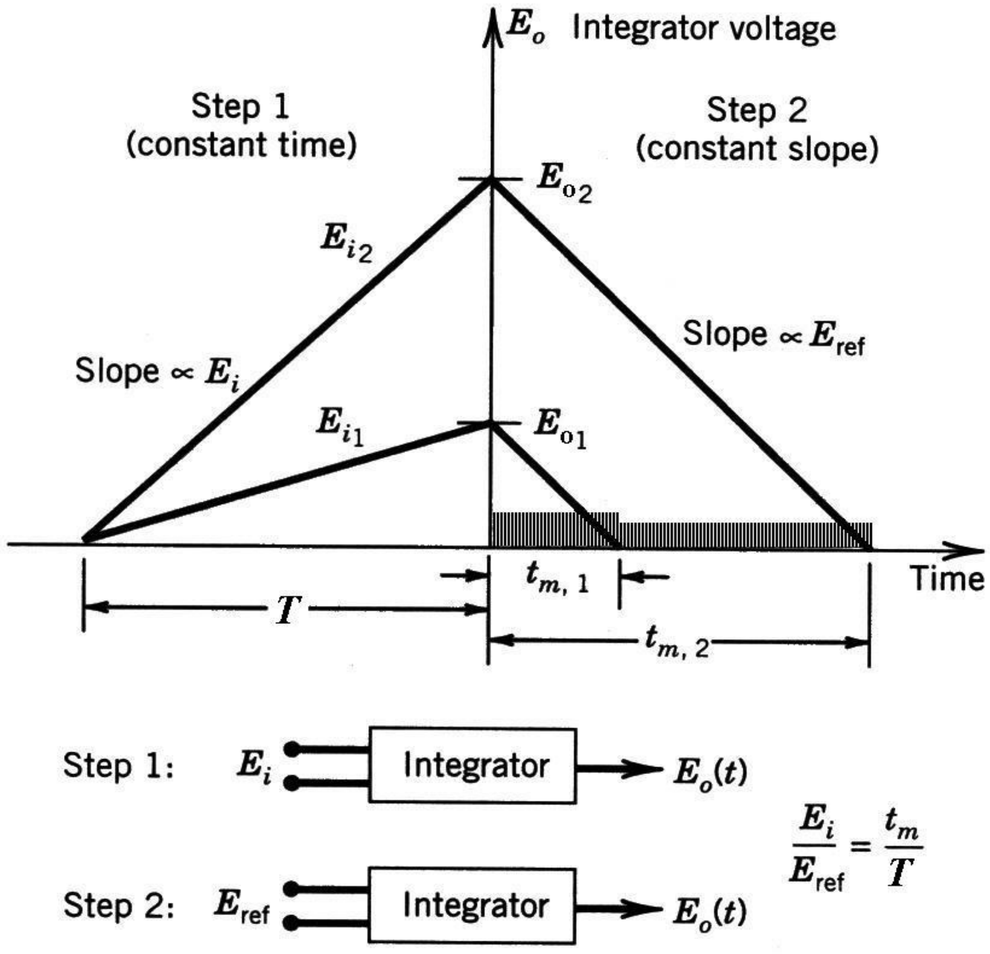
The analog signal v_i must be kept constant for all the time of the conversion; this task is performed by an external device the ***sample and hold circuit*** :



The logic unit connects the constant input signal v_i to the integrator for a predefined time T , the output voltage v_o will be:

$$V_o = -\frac{1}{CR}\int_0^T V_i dt = -\frac{V_i}{CR}\int_0^T dt = -\frac{V_i \cdot T}{CR} = -\frac{T}{CR}\cdot V_i$$

After the fixed time T , the logic unit switches the integrator input to an internal signal $-v_r$, always of the *opposite sign* of the input signal. Both signals v_i and $-v_r$ are constant and produce two ramps at the integrator output v_o …



Dual-ramp analog voltage to digital conversion.

The integrator output voltage v_o at time *T* reflects the charge the capacitor *C* has physically accumulated during that time, which is also the charge the same capacitor releases during the time t_m of the descending ramp:

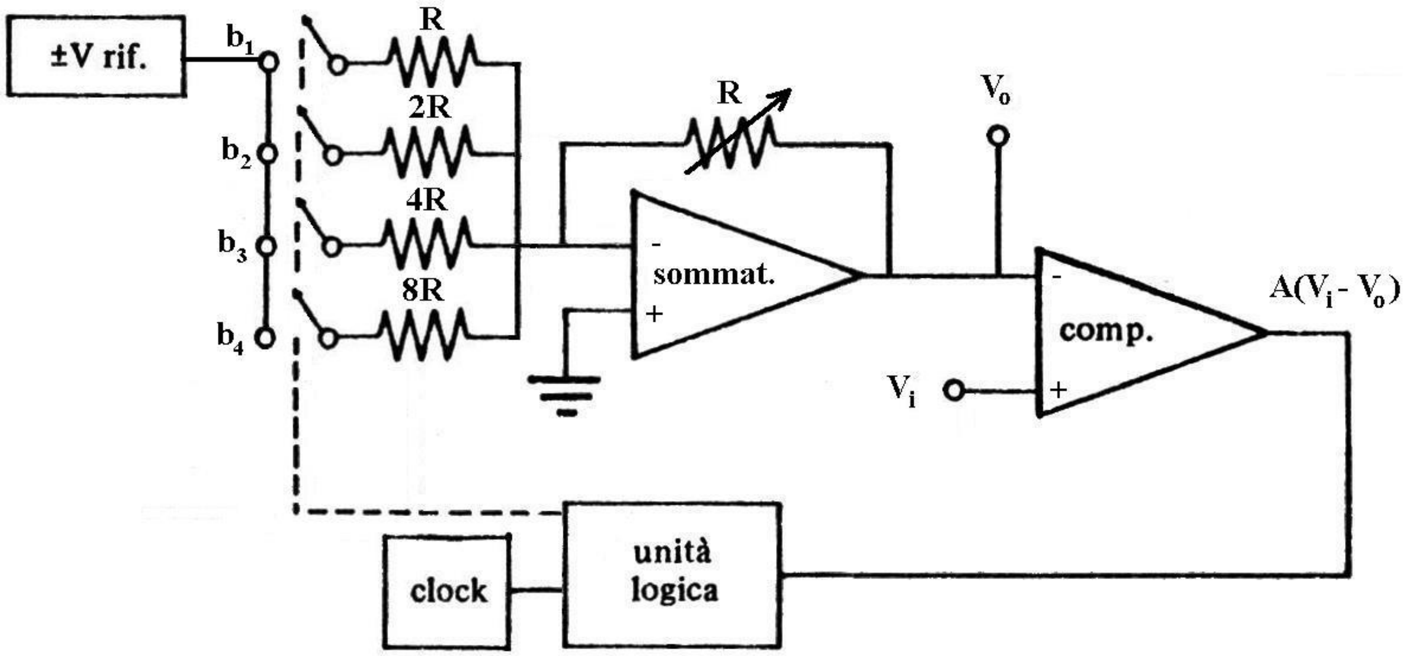
$$Q = V_i \cdot T = -V_r \cdot t$$

Therefore: $$\boxed{V_i = -\frac{V_r}{T} \cdot t}$$ which is the ***characteristic curve*** of the device !

Because v_r and *T* are constant for every input signal v_i, the signal v_i is simply proportional to the measured time t_m which, in fact, is different for each input voltage v_{i1}, v_{i2}, … The time t_m is measured by the *digital counter*, starting when the logic unit connects the internal reference signal and stopping when the "comparator signals to the logic unit" the integrator output v_o has crossed zero !

The ***sampling period*** is at least : $T + t_m$

Another ***A/D Converter***, employed in the digital acquisition systems, is the ***successive approximation converter*** :
A 4 bit example is shown in the figure here below:

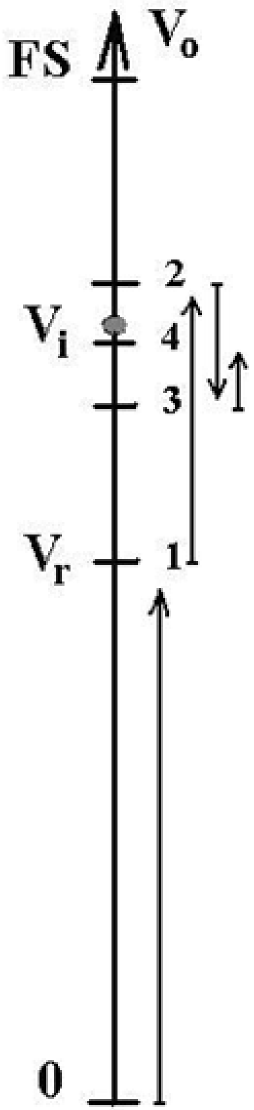


This converter is based on the *summing Operational Amplifier* and the working principle is based on comparing the input signal v_i with "successively added" internal reference voltages.
The logic unit operates successively on the switches $\boldsymbol{b_i}$ with i = 1, 2, … 4, which can assume the value **1** (close) or **0** (open).

The characteristic curve of the device is therefore:

$$V_o = R\left(\frac{b_1}{R}+\frac{b_2}{2R}+\frac{b_3}{4R}+\frac{b_4}{8R}\right)\cdot V_r = V_r\left(b_1+\frac{b_2}{2}+\frac{b_3}{4}+\frac{b_4}{8}\right)\frac{R}{R} = V_r\left(b_1+\frac{b_2}{2}+\frac{b_3}{2^2}+\frac{b_4}{2^3}\right)$$

The procedure goes step by step, as in the next example :



The input unknown signal to the device is V_i
at the beginning of the conversion, all switches are open

the characteristic curve is : $V_o = V_r\left(b_1 + \frac{b_2}{2} + \frac{b_3}{2^2} + \frac{b_4}{2^3}\right)$

the logic unit closes b_1 : it results $V_i > V_1$ the switch *remains* *__close__:* $b_1 = 1$
the logic unit closes b_2 : it results $V_i < V_2$ the switch *will be* *__reopened__:* $b_2 = 0$
the logic unit closes b_3 : it results $V_i > V_3$ the switch *remains* *__close__:* $b_3 = 1$
the logic unit closes b_4 : it results $V_i > V_4$ the switch *remains* *__close__:* $b_4 = 1$

where V_k $k = 1 \ldots 4$ is the summing OA output voltage at each step.

At the end of the “successive approximations” procedure we get :

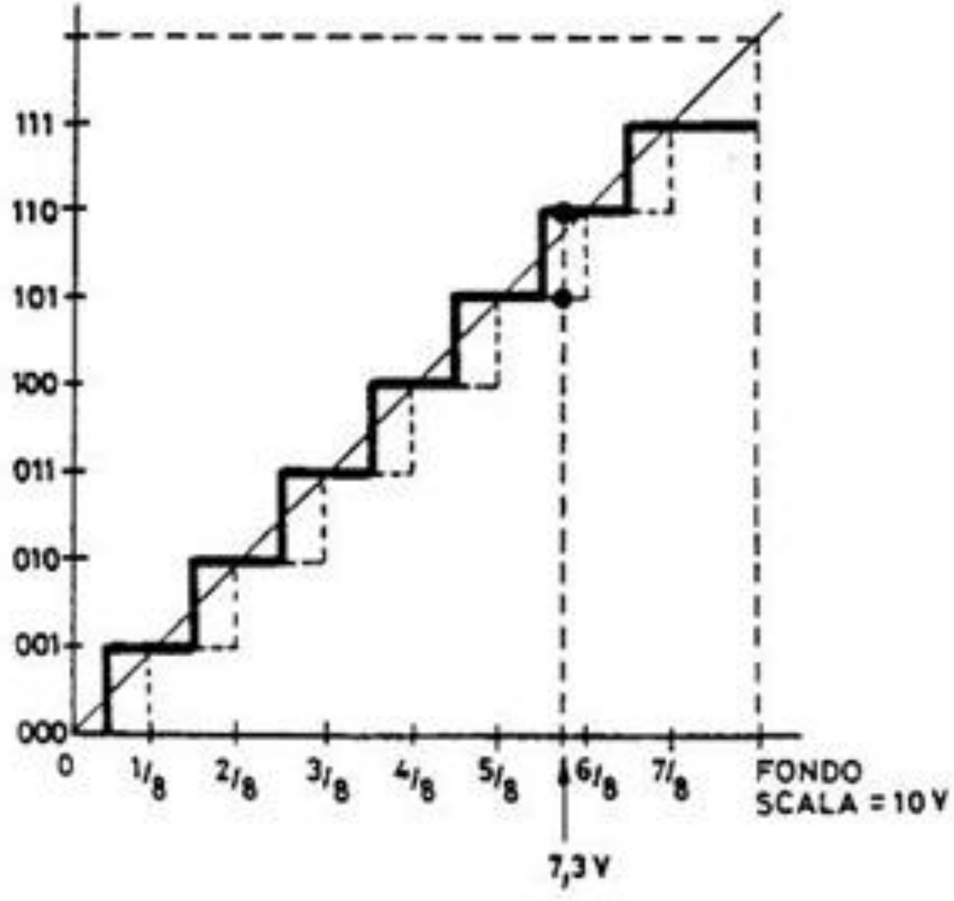
$V_o = V_4 = V_r\left(1 + \frac{0}{2} + \frac{1}{2^2} + \frac{1}{2^3}\right) = \frac{11}{8}V_r$ and the corresponding ***binary code*** is “1 0 1 1”

Note that the last step $V_o = V_4 \neq V_i$! There is a ***__discretization error__*** $\boxed{\varepsilon_d = V_i - V_4}$

The *discretization error* is due to the *limited number of switches* (***bits***) of the *A/D converter*, in fact the ***__resolution__*** of the device is equal to the LSB : $V_{FS}/2^4 = 2V_r/16$

Discretization error can be minimized only *adding more bits* (switches) to the A/D converter !
Modern A/D converter have at least *12 bits* or *16 bits*, which means $2^{16} - 1 = 65.536$ discretization levels !

Note also that *successive approximation converters* always *approximate by defect* the analog value, and to mitigate this problem the characteristic curve is shifted ½ LSB to the left, as shown below for a 3 bit converter :

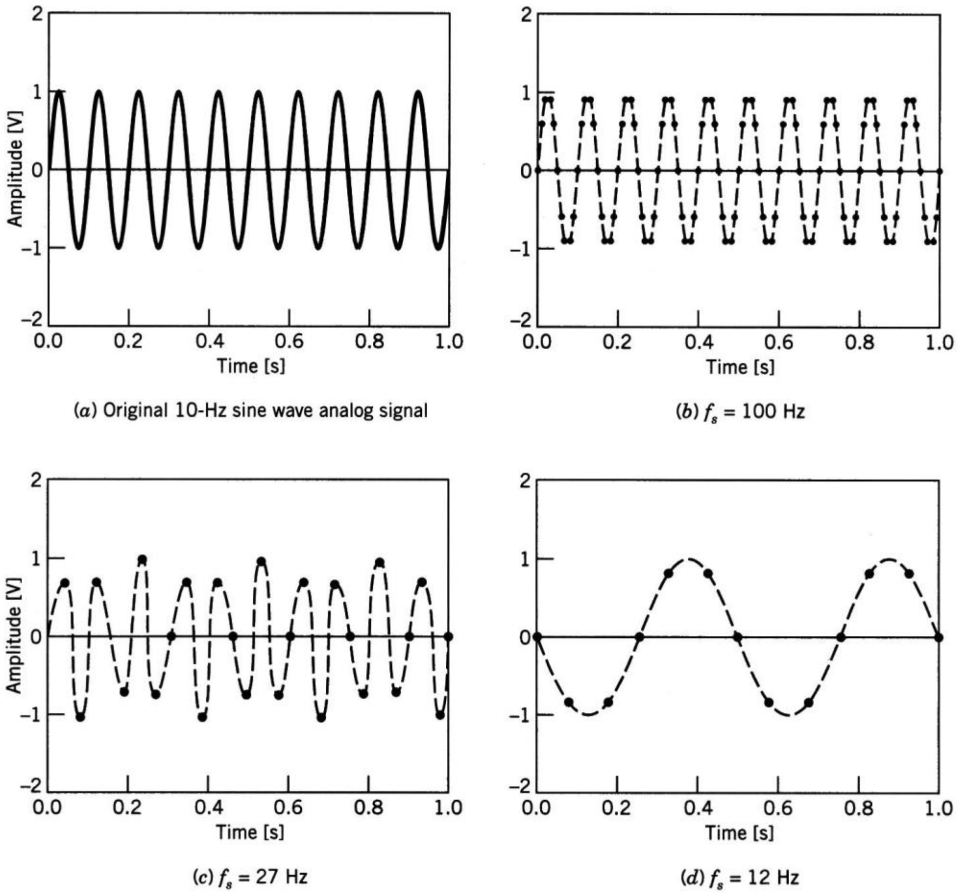


The figure show also another unavoidable error the A/D converters do, the ***saturation error*** : when all the bits (switches) are set to 1 the approximated output value is 7/8 of the Full Scale voltage or ***range*** : $V_{FS} = 2V_{ref}$.
This problem can be solved only by *increasing the range* of the A/D converter !

Successive approximation A/D converters have a fixed machine time to do the conversion therefore, the ***sampling period*** is dependent only on the number of successive approximations (*bits*) and is relatively short (a few *µs*), which makes this A/D converter a relatively fast device !

The *velocity of conversion* is directly related to the ***dynamic response*** of such devices :
If the conversion procedure is fats, the <u>*sampling period T_s can be short*</u> and the <u>*sampling frequency f_s can be high*</u> !

The ***<u>Nyquist sampling theorem</u>*** states that the *sampling frequency of the A/D converter must be at least double of the highest frequency of the signal* : $f_s \geq 2\, f_{Max}$
If this rule is not observed, the *discrete signal* will be affected by ***<u>aliasing</u>***:

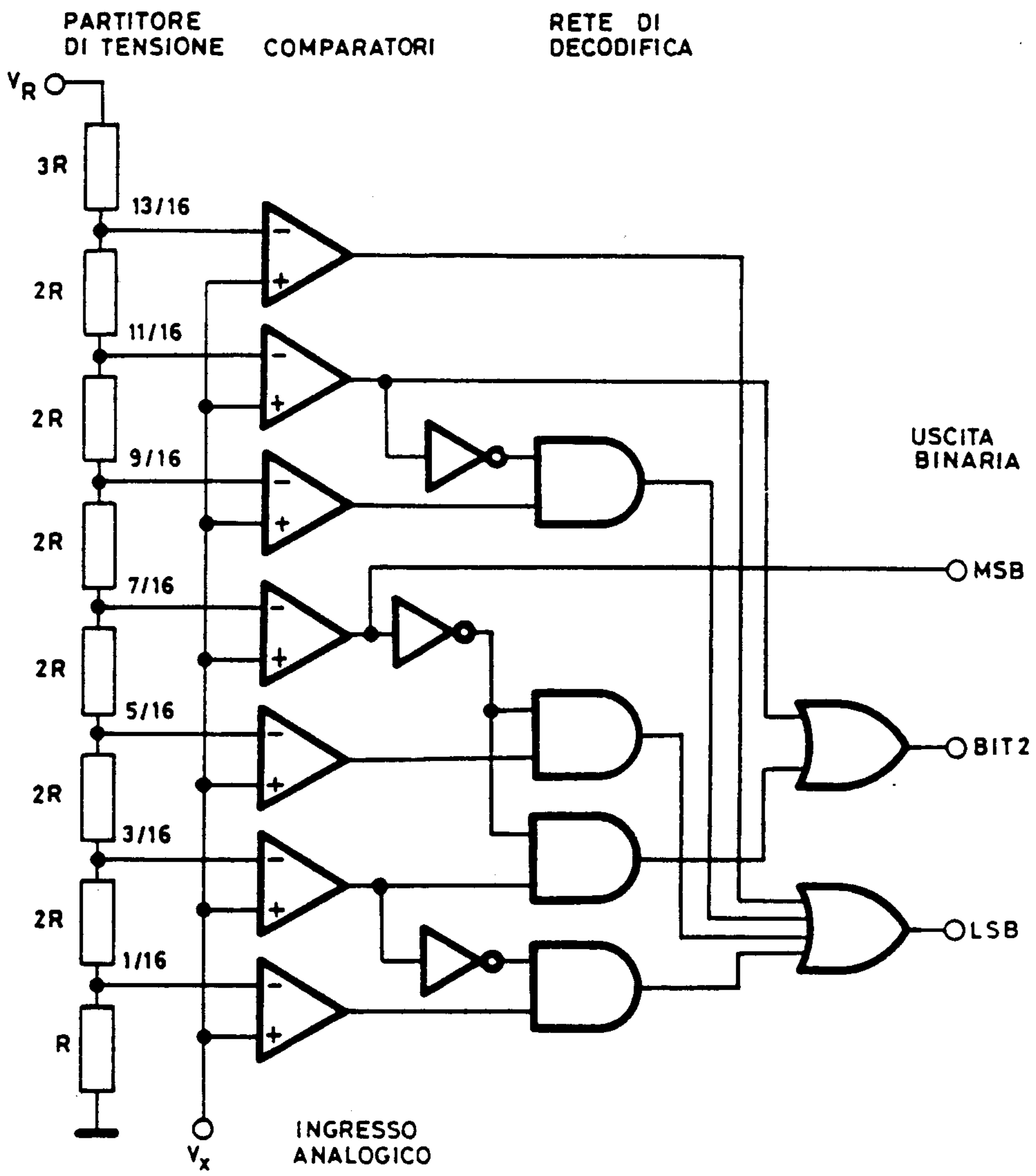


The effect of sample rate on signal frequency and amplitude interpretation.

Be advised that, to have a <u>good digital reconstruction of the analog waveform</u>, it is good practice to use a sampling frequency at leest 10 times higher than the signal highest frequency !

$$\boxed{f_s \geq 10\, f_{Max}}$$

The *fastest A/D converter* employed in measurement instrumentation (***digital oscilloscopes***) is the ***FLASH converter*** :



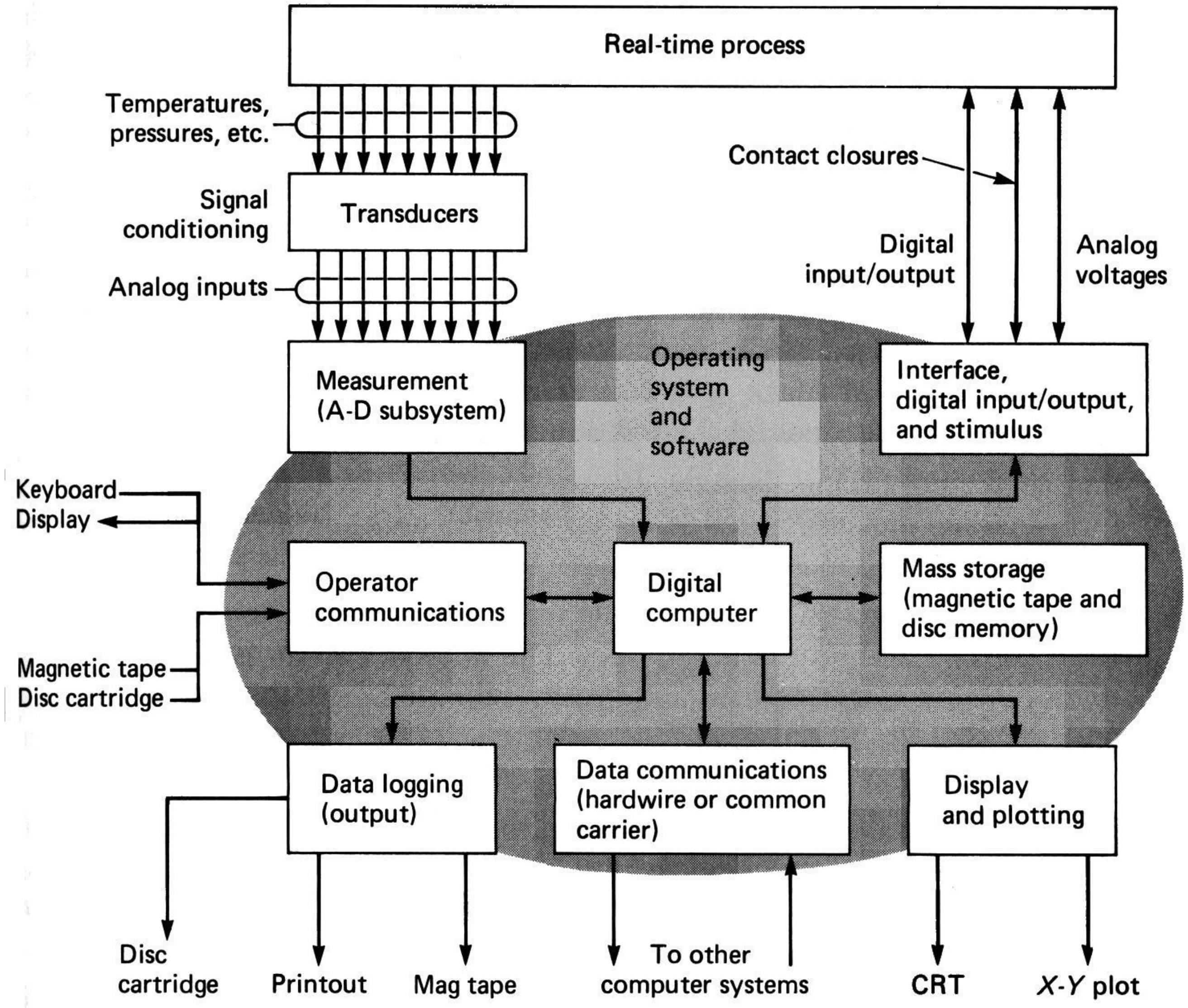
The *3 bit* example in the figure has $2^3 - 1 = 7$ comparators in the circuit.

The resistor network operates a "multiple voltage partition" from the *full range* V_r to *zero,* which are also the *quantization levels* of the device. The comparators put to 0 (**low**) the output if the input signal V_i is lower than the partitioned inner reference voltage V_r or to 1 (**high**) if the input signal V_i is higher than the corresponding partitioned voltage !

The comparators work in parallel and achieve all together the comparison. The codifying network reconstructs the binary code for the corresponding *input voltage level* !

Flash comparators are *incredibly fast* (*sampling period lower than 1 μs*) but are increasingly complicate when the number of bits increase: an *8 bit comparator requires $2^8 - 1 = 255$ comparators inside*.

Scheme of a modern digital data acquisition system



Electronics and *Information and Communication Technologies* have deeply entered the measurement world, leaving to physics only the first stage of the measurement chain: the ***transducer***, the only one in strict contact with the *measurand* …